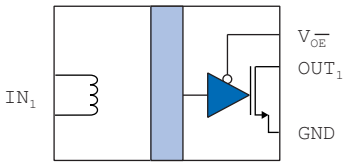
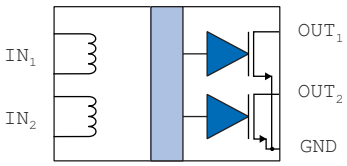
Passive-Input Digital Isolators – Open Drain Outputs

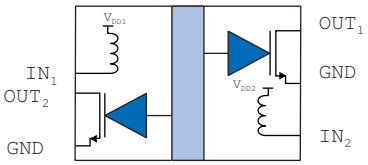
Functional Diagrams



IL610A



IL611A



IL612A

Features

- 10 Mbps data rate
- Flexible inputs with very wide input voltage range
- 5 mA input current
- Failsafe output (logic high output for zero coil current)
- No carrier or clock for low EMI emissions and susceptibility
- 3 V to 5 V power supplies
- 44000 year barrier life
- Low power dissipation
- –40 °C to 85 °C temperature range
- 2500 V_{RMS} isolation
- IEC 60747-17 (VDE 0884-17):2021-10; UL 1577
- 8-pin MSOP, SOIC, and PDIP packages

Applications

- General purpose optocoupler replacement
- Wired-OR alarms
- SPI interface
- I^2C
- RS-485, RS-422, or RS-232
- Space-critical multi-channel applications
- Isolated relays and actuators

Description

The IL600A-Series are isolated signal couplers with open-drain outputs. They have a similar interface but better performance and higher package density than optocouplers.

The devices are manufactured with NVE's patented* IsoLoop® spintronic Giant Magnetoresistive (GMR) technology for small size, high speed, and low power.

A unique ceramic/polymer composite barrier provides excellent isolation and virtually unlimited barrier life.

A resistor sets the input current; a capacitor in parallel with the current-limit resistor provides improved dynamic performance.

These versatile components simplify inventory requirements by replacing a variety of optocouplers, functioning over a wide range of data rates, edge speeds, and power supply levels. The devices are available in MSOP, SOIC, and PDIP packages, as well as bare die.

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Absolute Maximum Ratings(1)

Parameters	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Storage Temperature	T_S	–55(2)		150	°C	
Junction Temperature	T_J	–55		150	°C	
Ambient Operating Temperature	T_A	–40(3)		85	°C	
Supply Voltage	V_{DD}	–0.5		7	V	
DC Input Current	I_{IN}	–25		25	mA	
AC Input Current (Single-Ended Input)	I_{IN}	–35		35	mA	
AC Input Current (Differential Input)	I_{IN}	–75		75	mA	
Output Voltage	V_O	–0.5		V_{DD}+1.5	V	
Maximum Output Current	I_O	–10		10	mA	
ESD (IL610A Output Enable CMOS input)			2		kV	HBM

Note 1: Operating at absolute maximum ratings will not damage the device. Parametric performance is not guaranteed at absolute maximum ratings.
Note 2: -55ºC applies to all except IL611A-1E, IL611A-1ETR7 and IL611A-1ETR13. -20ºC applies to IL611A-1E, IL611A-1ETR7 and IL611A-1ETR13
Note 3: -40ºC applies to all except IL611A-1E, IL611A-1ETR7 and IL611A-1ETR13. -20ºC applies to IL611A-1E, IL611A-1ETR7 and IL611A-1ETR13

Recommended Operating Conditions

Parameters	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Ambient Operating Temperature	T_A	–40(3)		85	°C	
Junction Temperature	T_J	–40		100	°C	
Supply Voltage	V_{DD}	3.0		5.5	V	
Open Drain Reverse Voltage	V_{SD}	–0.5			V	
Open Drain Voltage	V_{DS}			6.5	V	
Open Drain Load Current	I_{OD}			7	mA	
Common Mode Input Voltage	V_{CM}			400	V_{RMS}	

Safety and Approvals

IEC 60747-17 (VDE 0884-17):2021-10 (Basic Isolation; VDE File Number 5016933-4880-0001):

- Isolation voltage (V_{ISO}): 2500 V_{RMS}
- Transient overvoltage (V_{IOTM}): 4000 V_{PK}
- Surge rating 4000 V
- Each part tested at 1590 V_{PK} for 1 second, 5 pC partial discharge limit
- Samples tested at 4000 V_{PK} for 60 sec.; then 1358 V_{PK} for 10 sec. with 5 pC partial discharge limit

- Working Voltage (V_{IORM}; pollution degree 2):

Package	Part No. Suffix	Working Voltage
MSOP8	-1	800 V_{RMS}
SOIC8	-3	700 V_{RMS}
PDIP8	-2	900 V_{RMS}

Safety-Limiting Values	Symbol	Value	Units
Safety rating ambient temperature	T_S	180	°C
Safety rating power (180°C)	P_S	270	mW
Supply current safety rating (total of supplies)	I_S	54	mA

UL 1577(Component Recognition Program File Number E207481)

- 2500 V rating for all types other than MSOP.
- Each part other than MSOP tested at 3000 V_{RMS} (4240 V_{PK}) for 1 second; each lot sample tested at2500 V_{RMS} (3530 V_{PK}) for 1 minute.
- MSOP rating 1000 V; tested at 1200 V_{RMS} (1768 V_{PK}) for 1 second; each lot sample tested at 1500 V_{RMS} (2121 V_{PK}) for 1 minute.

Soldering Profile

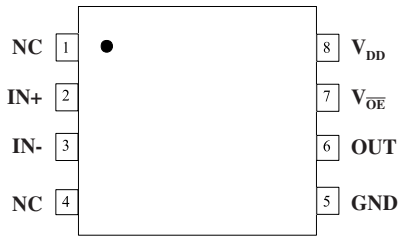
Per JEDEC J-STD-020C; MSL 1

Electrostatic Discharge Sensitivity

This product has been tested for electrostatic sensitivity to the limits stated in the specifications. However, NVE recommends that all integrated circuits be handled with appropriate care to avoid damage. Damage caused by inappropriate handling or storage could range from performance degradation to complete failure.

IL610A Pin Connections

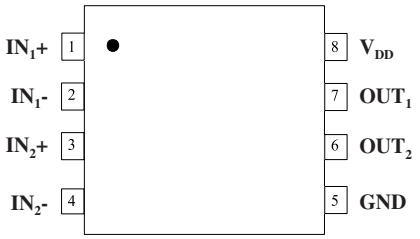
1	NC	No internal connection
2	IN+	Coil connection
3	IN–	Coil connection
4	NC	No internal connection
5	GND	Ground return for V_{DD}
6	OUT	Data out
7	$V_{\overline{OE}}$	Output enable. Internally held low with 100 kΩ
8	V_{DD}	Supply Voltage



IL610A

IL611A Pin Connections

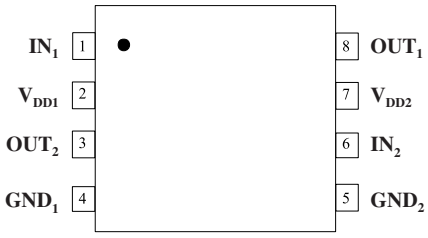
1	IN_1+	Channel 1 coil connection
2	$IN_1–$	Channel 1 coil connection
3	IN_2+	Channel 2 coil connection
4	$IN_2–$	Channel 2 coil connection
5	GND	Ground return for V_{DD}
6	OUT_2	Data out, channel 2
7	OUT_1	Data out, channel 1
8	V_{DD}	Supply Voltage



IL611A

IL612A Pin Connections

1	IN_1	Data in, channel 1
2	V_{DD1}	Supply Voltage 1
3	OUT_2	Data out, channel 2
4	GND_1	Ground return for V_{DD1}
5	GND_2	Ground return for V_{DD2}
6	IN_2	Data in, channel 2
7	V_{DD2}	Supply Voltage 2
8	OUT_1	Data out, channel 1



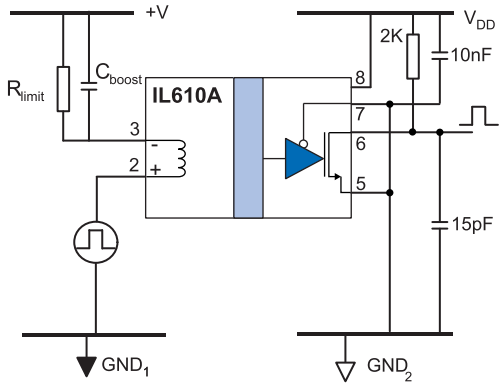
IL612A

Operating Specifications

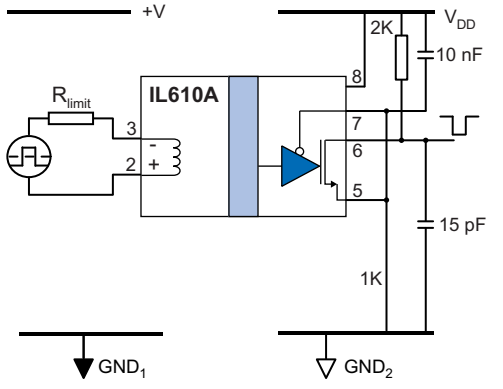
Input Specifications (V_{DD} = 3 V – 5.5 V; T = –40°C[2] – 85°C unless otherwise stated)						
Parameters	**Symbol**	**Min.**	**Typ.**	**Max.**	**Units**	**Test Conditions**
Coil Input Resistance	R_{COIL}	47	85	112	Ω	T = 25°C
		31	85	128	Ω	T = –40°C – 85°C
Coil Resistance Temperature Coefficient	TC R_{COIL}		0.2	0.25	Ω/°C	
Coil Inductance	L_{COIL}		9		nH	
DC Input Threshold (5 V)	I_{INH-DC}	0.5	1		mA	Test Circuit 1; V_{DD} = 4.5 V – 5.5 V
	I_{INL-DC}		3.5	5	mA	
DC Input Threshold (3 V)	I_{INH-DC}		0.5	0.3	mA	Test Circuit 1; V_{DD} = 3V – 3.6 V; no boost cap
	I_{INL-DC}		5	8	mA	
Dynamic Input Threshold (3 V)	$I_{INH-BOOST}$	0.5	1		mA	V_{DD} = 3V – 3.6 V; t_{IR} = t_{IF} = 3 ns; C_{BOOST} = 16 pF
	$I_{INL-BOOST}$		3.5	5	mA	
Differential Input Threshold	$I_{INH-DIFF}$	0.5	1		mA	Test Circuit 2; V_{DD} = 3V – 5.5 V; input current reverses; boost cap not required
	$I_{INL-DIFF}$		3.5	5	mA	
Failsafe Input Current[1] (5 V)	$I_{FS-HIGH}$	–25		0.5	mA	Test Circuit 1; V_{DD} = 4.5 V – 5.5 V
	I_{FS-LOW}	5		25	mA	
Failsafe Input Current[1] (3 V)	$I_{FS-HIGH}$	–25		0.3	mA	Test Circuit 1; V_{DD} = 3 V – 3.6 V
	I_{FS-LOW}	8		25	mA	
V_{OE} Logic High Input Voltage	V_{IH}	2.4		V_{DD1}	V	
V_{OE} Logic Low Input Voltage	V_{IL}	0		0.8	V	
Input Signal Rise and Fall Times	t_{IR}, t_{IF}			1	µs	
Common Mode Transient Immunity	$\|CM_H\|$,$\|CM_L\|$	15	20		kV/µs	V_T = 300 V_{peak}

Notes:

1. Failsafe Operation is defined as the guaranteed output state which will be achieved if the DC input current falls between the input levels specified (see Test Circuit 1 for details). Note if Failsafe to Logic Low is required, the DC current supplied to the coil must be at least 8 mA using 3.3 V supplies versus 5 mA for 5 V supplies.
2. -20ºC for IL611A-1E, IL611A-1ETR7 and IL611A-1ETR13



Test Circuit 1 (Single-Ended)



Test Circuit 2 (Differential)

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Electrical Specifications (V_{DD} = 3 V – 5.5 V; T = –40°C[3] – 85°C unless otherwise stated)						
Parameters	**Symbol**	**Min.**	**Typ.**	**Max.**	**Units**	**Test Conditions**
Quiescent Supply Current (5 V)						
IL610A	I_{DD}		2	3	mA	V_{DD} = 5 V, I_{IN}=0 R_{pullup} = open circuit
IL611A	I_{DD}		4	6	mA	
IL612A	I_{DD1}		2	3	mA	
IL612A	I_{DD2}		2	3	mA	
Quiescent Supply Current (3.3 V)						
IL610A	I_{DD}		1.3	2	mA	V_{DD}= 3.3 V, I_{IN}=0 R_{pullup} = open circuit
IL611A	I_{DD}		2.6	4	mA	
IL612A	I_{DD1}		1.3	2	mA	
IL612A	I_{DD2}		1.3	2	mA	
Logic High Output Voltage[1]	V_{OH}		V_{DD}		V	Off State
Logic Low Output Voltage	V_{OL}		0	0.1	V	I_O = –20 µA
			0.4	0.8	V	I_O = –4 mA
Logic Output Current	$\|I_O\|$	7	10		mA	

Switching Specifications (V_{DD} = 3 V – 5.5 V; T = –40°C[3] – 85°C unless otherwise stated)						
Parameters	**Symbol**	**Min.**	**Typ.**	**Max.**	**Units**	**Test Conditions**
Input Signal Rise and Fall Times	t_{IR}, t_{IF}			10	µs	Test Circuit 1; t_{IR} = t_{IF} = 3 ns; C_{BOOST} = 16 pF
Data Rate		10			Mbps	
Minimum Pulse Width	PW	100			ns	
Propagation Delay Input to Output (High to Low)	t_{PHL}		20	25	ns	
Propagation Delay Input to Output (Low to High)	t_{PLH}		50	75	ns	

Notes:

1. V_{DD} refers to the supply voltage on the output side of the isolated channel.
2. Failsafe Operation is defined as the guaranteed output state which will be achieved if the DC input current falls between the input levels specified (see Test Circuit 1 for details). Note if Failsafe to Logic Low is required, the DC current supplied to the coil must be at least 8 mA using 3.3 V supplies versus 5 mA for 5 V supplies.
3. -20ºC for IL611A-1E, IL611A-1ETR7 and IL611A-1ETR13

Insulation Specifications

Parameters		Symbol	Min.	Typ.	Max.	Units	Test Conditions
Creepage Distance (external)							
MSOP			3.01			mm	
SOIC			4.03			mm	
PDIP			7.08			mm	
Total Barrier Thickness			0.012	0.013		mm	
Leakage Current				0.2		µA	240 V_{RMS}, 60 Hz
Barrier Resistance		R_{IO}		$>10^{14}$		Ω	500 V
Barrier Capacitance		C_{IO}		7		pF	f = 1 MHz
Comparative Tracking Index		CTI	≥175			V	Per IEC 60112
High Voltage Endurance (Maximum Barrier Voltage for Indefinite Life)	AC	V_{IO}	1000			V_{RMS}	At maximum operating temperature
	DC		1500			V_{DC}	
Barrier Life				44000		Years	100°C, 1000 V_{RMS}, 60% CL activation energy

Thermal Characteristics

Parameter		Symbol	Min.	Typ.	Max.	Units	Test Conditions
Junction–Ambient Thermal Resistance	MSOP SOIC PDIP	θ_{JA}		184 134 114		°C/W	Double-sided PCB in free air
Junction–Case (Top) Thermal Resistance	MSOP SOIC PDIP	θ_{JC}		15 10 36			
Power Dissipation	MSOP SOIC PDIP	P_D			500 675 800	mW	

Applications Information

IL600-Series Isolators are current mode devices. As shown in Figure 1, current flow into the input coil results in an output logic low (output pulled to ground), and zero input current results in an output logic high (the open drain state).

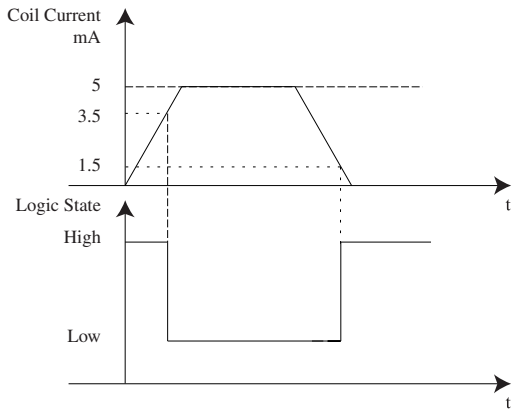


Figure 1. Typical IL600-Series Transfer Function

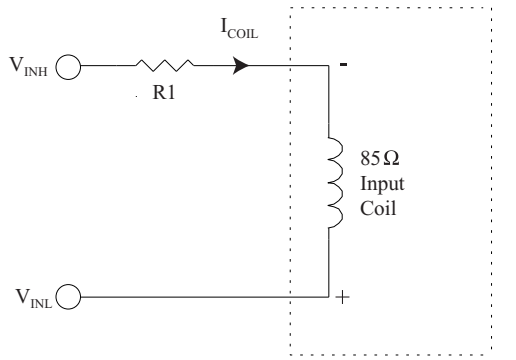


Figure 2. Limiting Resistor Calculation Equivalent Circuit

Coil Polarity

The device switches to logic low if current flows from (In−) to (In+). ***Note that the designations "In−" and "In+" refer to logic levels, not current flow.*** Positive values of current mean current flow into the In− input.

Input Resistor Selection

Resistors set the coil input current (see Figure 2). There is no limit to input voltages because there are no semiconductor input structures.

Worst-case logic low threshold current is 8 mA, which is for single-ended operation with a 3 V supply. In differential mode, where the input current reverses, the logic low threshold current is 5 mA for the range of supplies. A "boost capacitor" creates current reversals at edge transitions, reducing the input logic low threshold current to the differential level of 5 mA.

Typical Resistor Values

V_{COIL}	Coil Resistor
3.3 V	510 Ω
5 V	820 Ω

The table shows typical values for the external resistor for 5 mA coil current. The values are approximate and should be adjusted for temperature or other application specifics.

Single-Ended or Differential Input

Inputs can be single-ended or differential (see Test Circuits on page 5). In the differential mode, current will naturally flow through the coil in both directions without a boost capacitor, although the capacitor can still be used for increased external field immunity or improved PWD.

Absolute Maximum recommended coil current in single-ended mode is 25 mA while differential mode allows up to ±75 mA to flow. The difference in specifications is due to the risk of electromigration of coil metals under constant current flow. In single ended mode, long-term DC current flow above 25 mA can cause erosion of the coil metal. In differential mode, erosion takes place in both directions as each current cycle reverses and has a net effect of zero up to the absolute maximum current.

An advantage over optocouplers and other high-speed couplers in differential mode is that no reverse bias protection for the input structure is required for a differential signal.

One of the more common applications is for an isolated Differential Line Receiver. For example, RS-485 can drive an IL610 directly for a fraction of the cost of an isolated RS-485 node (see *Illustrative Applications*).

Non-inverting and Inverting Configurations

IL600-Series Isolators can be configured in non-inverting and inverting configurations (see Figure 3). In a typical non-inverting circuit, the In– terminal is connected via a 1 kΩ input resistor to the supply rail, and the input is connected to the In+ terminal. The supply voltage is +5 V and the input signal is a 5 V CMOS signal. When a logic high (+5 V) is applied to the input, the current through the coil is zero. When the input is a logic low (0 V), at least 5 mA flows through the coil from the In– side to the In+ side.

The inverting configuration is similar to standard logic. In the inverting configuration, the signal into the coil is differential with respect to ground. The designer must ensure that the difference between the logic low voltage and the coil ground is such that the residual coil current is less than 0.5 mA.

IL612A inputs that do not offer inverting operation since the coil In– input is hardwired internally to the device power supply. Therefore, it is important to ensure the isolator power supply is at the same voltage as the power supply to the source of the input logic signal.

Both single ended and differential inputs can be handled without reverse bias protection.

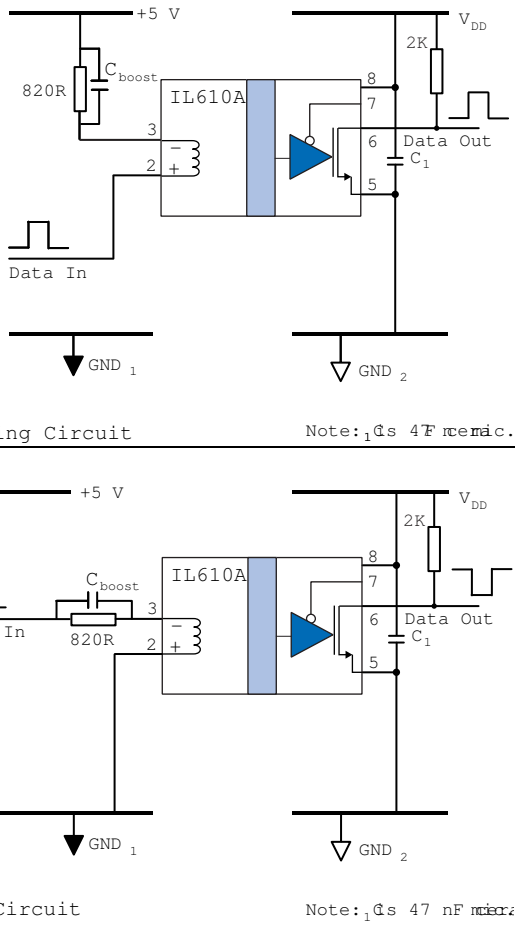


Figure 3. Non-inverting and inverting circuits

Boost Capacitor

The boost capacitor in parallel with the current-limiting resistor boosts the instantaneous coil current at the signal transition. This ensures switching and reduces propagation delay and reduces pulse-width distortion.

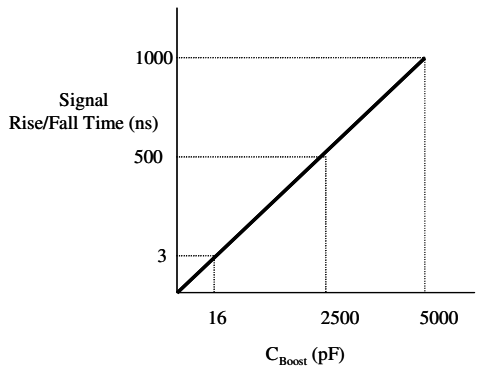


Figure 4. C_{boost} Selector

Select the value of the boost capacitor based on the rise and fall times of the signal driving the inputs. The instantaneous boost capacitor current is proportional to input edge speeds ($C\frac{dV}{dt}$). Select a capacitor value based on the rise and fall times of the input signal to be isolated that provides approximately 20 mA of additional "boost" current. Figure 4 is a guide to boost capacitor selection. For high-speed logic signals (t_r,t_f < 10 ns), a 16 pF capacitor is recommended. The capacitor value is generally not critical; if in doubt, choose a higher value.

Dynamic Power Consumption

Power consumption is proportional to duty cycle, not data rate. The use of NRZ coding minimizes power dissipation since no additional power is consumed when the output is in the high state. In differential mode, where the logic high condition may still require a current to be forced through the coil, power consumption will be higher than a typical NRZ single ended configuration.

Power Supply Decoupling

0.1 µF typical (0.047 µF minimum) ceramic capacitors are recommended to decouple the power supplies. The capacitors should be placed as close as possible to the appropriate V_{DD} pin.

Maintaining Creepage

Creepage distances are often critical in isolated circuits. In addition to meeting JEDEC standards, NVE isolator packages have unique creepage specifications. Standard pad libraries often extend under the package, compromising creepage and clearance. Similarly, ground planes, if used, should be spaced to avoid compromising clearance. Package drawings and recommended pad layouts are included in this datasheet.

Electromagnetic Compatibility and Magnetic Field Immunity

Because IL600-Series Isolators are completely static, they have the lowest emitted noise of any non-optical isolators.

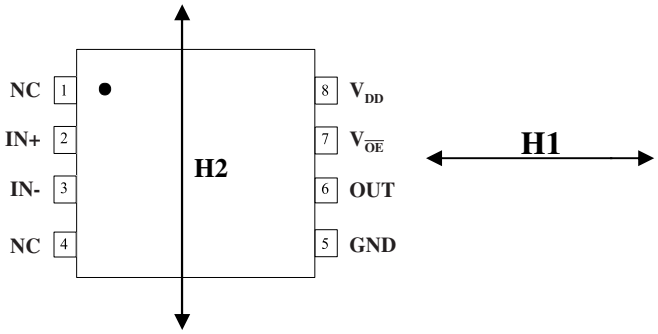
IsoLoop Isolators operate by imposing a magnetic field on a GMR sensor, which translates the change in field into a change in logic state. A magnetic shield and a Wheatstone Bridge configuration provide good immunity to external magnetic fields.

Immunity to external magnetic fields can be enhanced by proper orientation of the device with respect to the field direction, the use of differential signaling, and boost capacitors.

1. Orientation of the device with respect to the field direction

An applied field in the "H1" direction is the worst case for magnetic immunity. In this case the external field is in the same direction as the applied internal field. In one direction it will tend to help switching; in the other it will hinder switching. This can cause unpredictable operation.

An applied field in direction "H2" has considerably less effect and results in higher magnetic immunity.



2. Differential Signaling and Boost Capacitors

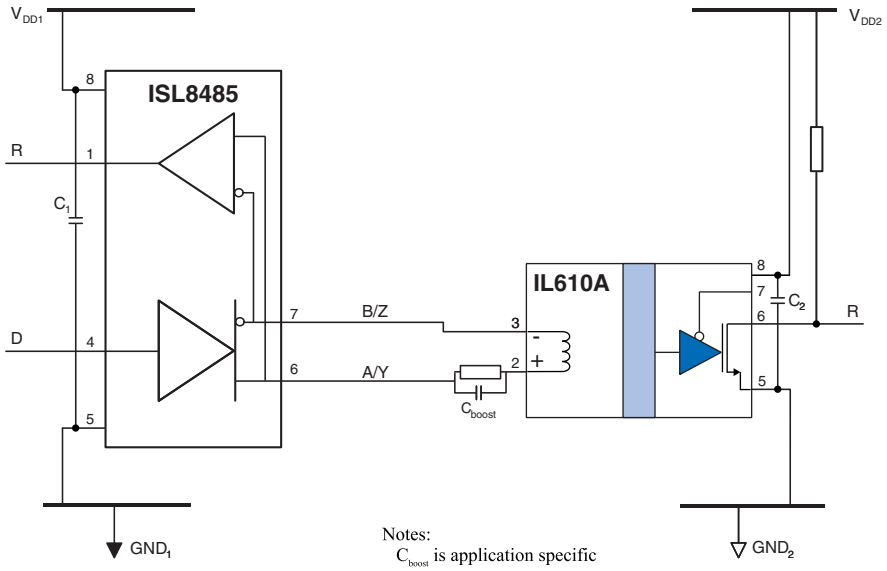
Regardless of orientation, driving the coil differentially improves magnetic immunity. This is because the logic high state is driven by an applied field instead of zero field, as is the case with single-ended operation. The higher the coil current, the higher the internal field, and the higher the immunity to external fields. Optimal magnetic immunity is achieved by adding the boost capacitor.

Method	Approximate Immunity	Immunity Description
Field applied in H1 direction	±20 Gauss	A DC current of 16 A flowing in a conductor 1 cm from the device could cause disturbance.
Field applied in H2 direction	±70 Gauss	A DC current of 56 A flowing in a conductor 1 cm from the device could cause disturbance.
Field applied in any direction but with boost capacitor (16 pF) in circuit	±250 Gauss	A DC current of 200 A flowing in a conductor 1 cm from the device could cause disturbance.

Data Rate and Magnetic Field Immunity

It is easier to disrupt an isolated DC signal with an external magnetic field than it is to disrupt an isolated AC signal. Similarly, a DC magnetic field will have a greater effect on the device than an AC magnetic field of the same effective magnitude. For example, signals with pulses longer than 100 µs are more susceptible to magnetic fields than shorter pulse widths.

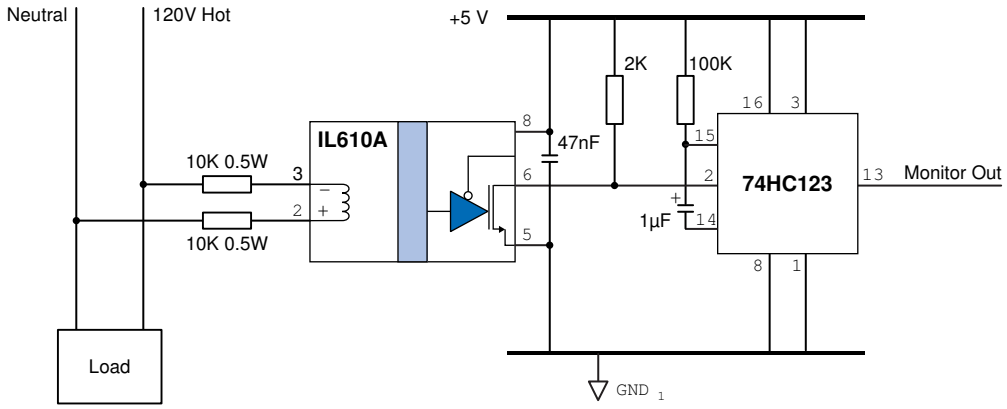
Illustrative Applications



Isolated RS-485 and RS-422 Receivers Using IL610As

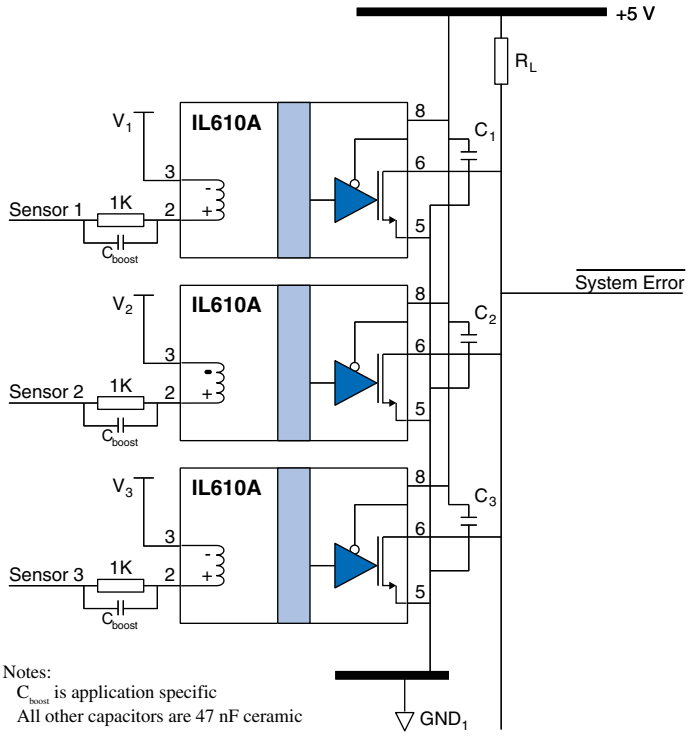
IL610As can be used as simple isolated RS-485 or RS-422 receivers, terminating signals at the IL610A for a fraction of the cost of an isolated node. Cabling is greatly simplified by eliminating the need to power the input side of the receiving board. No current-limiting resistor is needed for a single receiver because it will draw less current than the driver maximum. Current limiting resistors allow at least eight nodes without exceeding the maximum load of the transceiver chip. Placement of the current-limiting resistors on both lines provides better dynamic signal balance. There is no need for line termination resistors because the IL610A coil resistance of approximately 85 Ω is close to the characteristic impedance of most cables. The circuit is intrinsically open circuit failsafe because the IL610A is guaranteed to switch to the high state when the coil input current is less than 500 µA. For higher speed, a faster output device (such the CMOS-output IL600-Series Isolators) are needed as well as possibly better impedance matching.

Number of Nodes	Current Limit Resistors (Ω)
1	None
2	17
3	22
4	27
5	27
6	2
7	30
8	30



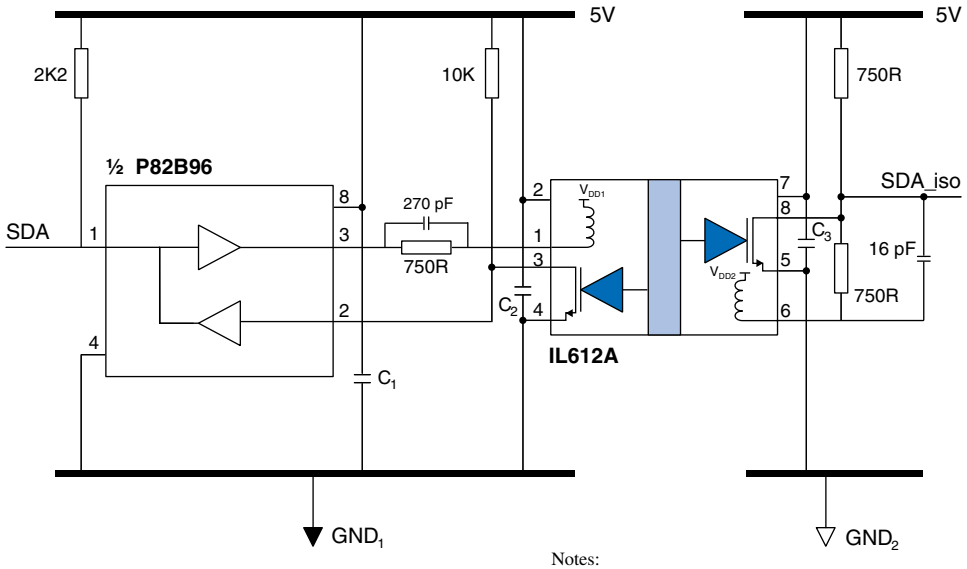
Isolated 120V Line Monitor

The wide input voltage range of IL600 Isolators allows connection to line voltage through current-limiting resistors. Unlike optocouplers, input voltage can reverse without damaging the inputs. In this illustrative circuit, "Monitor Out" goes low when line voltage drops significantly. The 74HC123 monostable converts the 60 Hz isolator output to a monitor signal.



Multi-channel Isolated Alarm Monitor

The open-drain outputs of IL600A-Series Isolators allow wired-OR outputs. The inputs can be configured for inverting or non-inverting operation (see Applications Information), and a very wide input voltage range is possible. This illustrative circuit provides fail-safe output (logic high output for zero coil current) and typical logic output sink current of 10 mA for each isolator.



Notes:
C1, C2, and C3 are 47nF ceramic
Resistor values change for 3 V operation

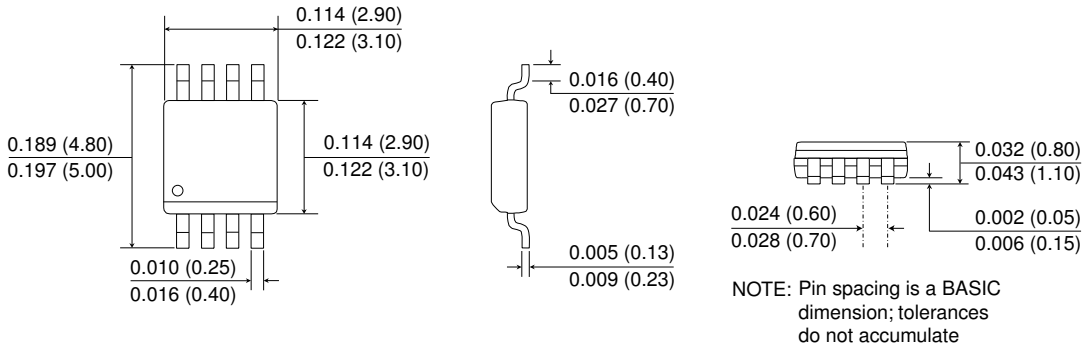
Isolation of I²C Nodes

This circuit provides bidirectional isolation of I²C bus signals with no restrictions on data rate and none of the I²C bus latch-up problems common with other isolation circuits. The SCL section is similar as shown in the schematic using the other half of the P82B96.

Package Drawings

8-pin MSOP (-1 suffix)

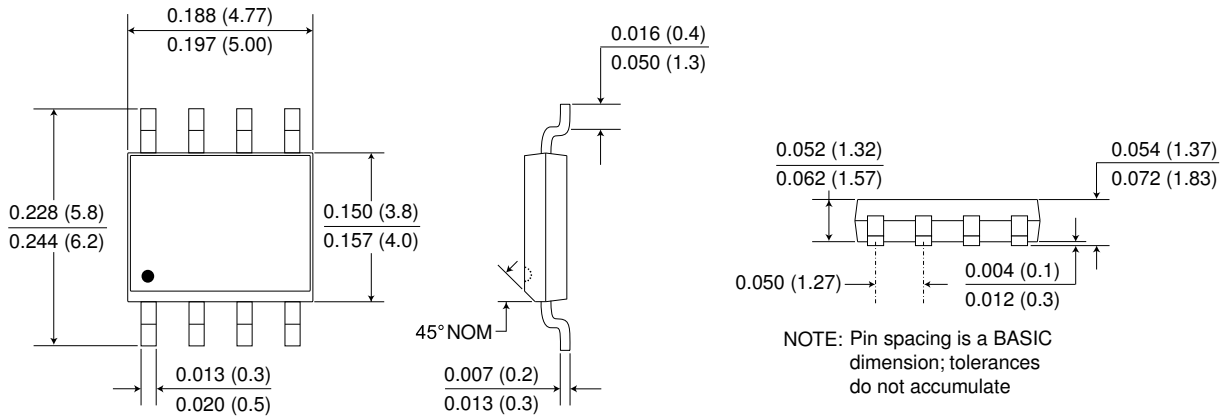
Dimensions in inches (mm); scale = approx. 5X



NOTE: Pin spacing is a BASIC dimension; tolerances do not accumulate

8-pin SOIC Package (-3 suffix)

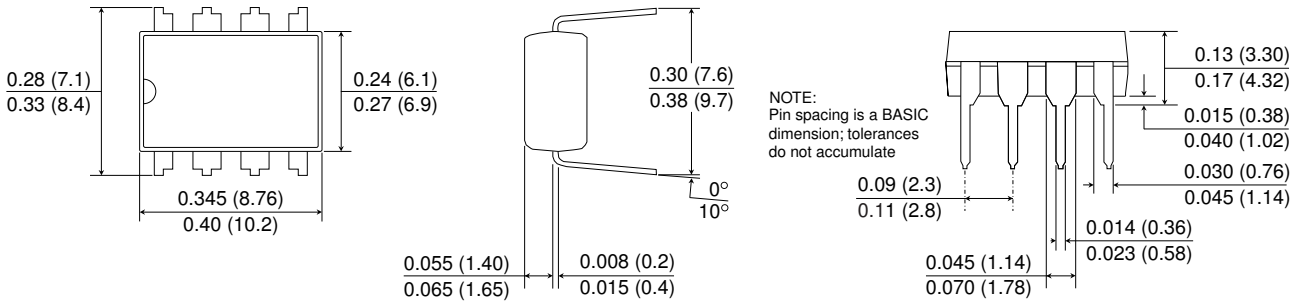
Dimensions in inches (mm); scale = approx. 5X



NOTE: Pin spacing is a BASIC dimension; tolerances do not accumulate

8-pin PDIP (-2 suffix)

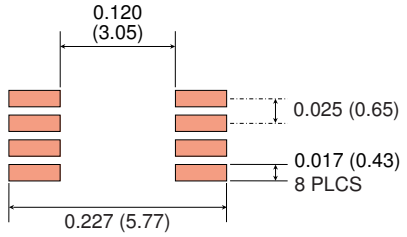
Dimensions in inches (mm); scale = approx. 2.5X



Recommended Pad Layouts

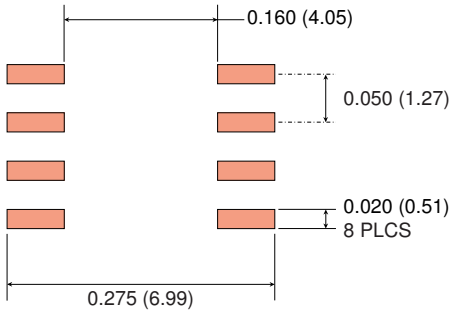
8-pin MSOP Pad Layout

Dimensions in inches (mm); scale = approx. 5X

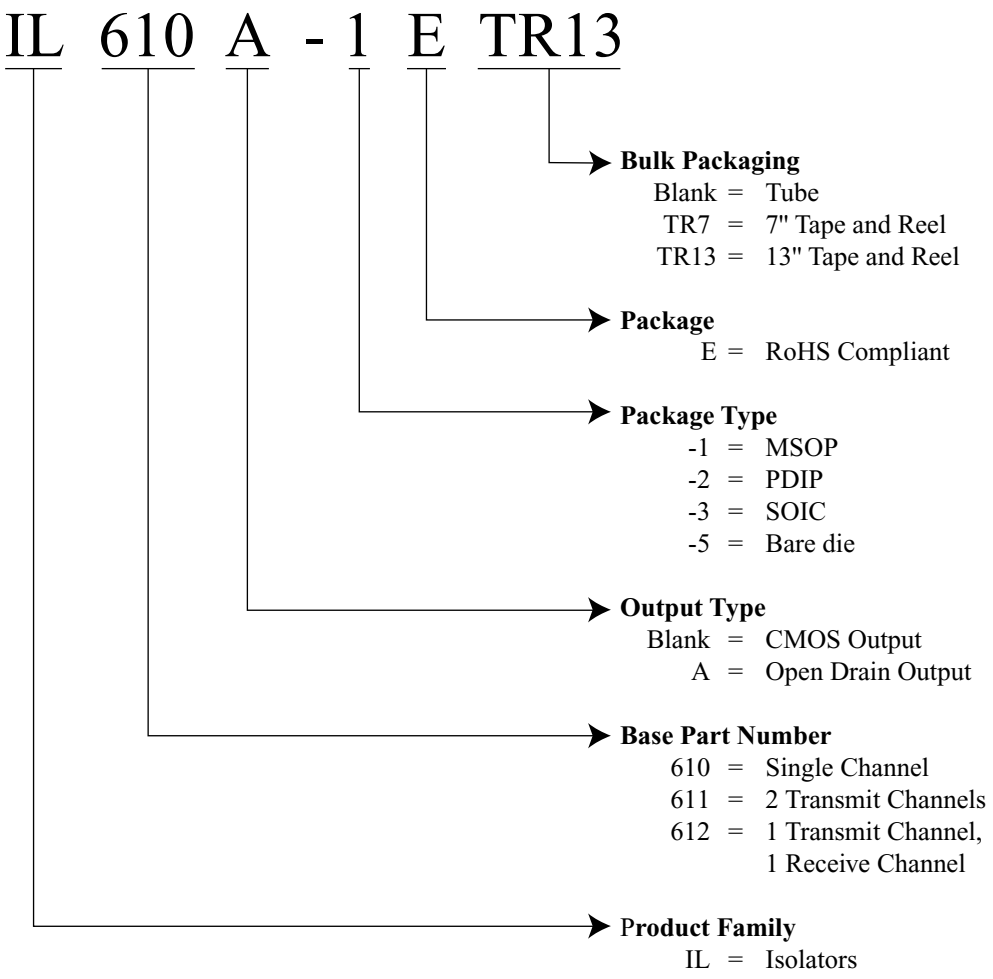


8-pin SOIC Pad Layout

Dimensions in inches (mm); scale = approx. 5X



Ordering Information and Valid Part Numbers



IL610A Valid Part Numbers

IL610A-1E
IL610A-2E
IL610A-3E
IL610A-5
IL610A-1ETR7
IL610A-3ETR7
IL610A-1ETR13
IL610A-3ETR13

IL611A Valid Part Numbers

IL611A-1E
IL611A-2E
IL611A-3E
IL611A-1ETR7
IL611A-3ETR7
IL611A-1ETR13
IL611A-3ETR13

IL612A Valid Part Numbers

IL612A-2E
IL612A-3E
IL612A-3ETR7
IL612A-3ETR13

RoHS COMPLIANT

Revision History

ISB-DS-001-IL600A-AC
Jan. 2023

Changes
- Clarified output states (p. 8).
- Clarified IL612A operation (p. 9).

ISB-DS-001-IL600A-AB

Changes
- Upgrade to VDE 0884-17 (p. 3).
- Increased Working Voltage ratings based on latest VDE testing (p. 3).
- Added VOE logic high and low input voltage specifications (p. 5).
- Added thermal characteristics (p. 7).

ISB-DS-001-IL600A-AA

Changes
- Corrected 8-pin SOIC package outline dimensions.
- Changed low temperature specification for IL611A-1E, IL611A-1ETR7 and IL611A-1ETR13.

ISB-DS-001-IL600A-Z

Changes
- IEC 60747-5-5 (VDE 0884) certification.
- Upgraded from MSL 2 to MSL 1.
- Rearranged input threshold specifications so maximum is more than minimum.

ISB-DS-001-IL600A-Y

Changes
- Added VDE 0884 pending.
- Added monostable to line monitor circuit (p. 11).
- Clarified circuit polarities.
- Updated package drawings.
- Added recommended solder pad layouts (p. 14).

ISB-DS-001-IL600A-X

Change
- Detailed isolation and barrier specifications.

ISB-DS-001-IL600A-W

Change
- Clarified Test Circuit 2 differential operation diagram (p.4).

ISB-DS-001-IL600A-V

Changes
- Separated and clarified Input Specifications.
- Added minimum/maximum coil resistance specifications.
- Merged and simplified “Operation” and “Applications” sections.

ISB-DS-001-IL600A-U

Change
- Update terms and conditions.

ISB-DS-001-IL600A-T

Change
- Additional changes to pin spacing specification on MSOP package drawing.

ISB-DS-001-IL600A-S

Change
- Changed pin spacing specification on MSOP package drawing.

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ISB-DS-001-IL600A-AC

January 2023